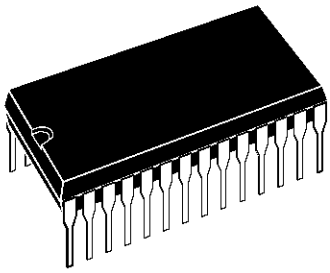
SGS-THOMSON MICROELECTRONICS

ST7291

8-BIT MCU WITH 16/24/32K ROM, TIMER, POWER SUPPLY SUPERVISOR AND CARRIER FREQUENCY GENERATOR

FUNCTIONAL DESCRIPTION

- 3 to 5.5V Supply Operating Range
- 8MHz Maximum Clock Frequency
- Fully Static operation
- 0 to +70°C Operating Temperature Range
- Run, Wait, Stop and RAM Retention modes
- User ROM: 16/24/32 Kbytes
- Data RAM: 256/384 bytes
- 28 pin Dual-in-Line and SO plastic packages
- 20 Bidirectional I/O lines
- 8 Interrupt Wake-Up programmable input lines
- 16-bit Timer with Output Compare (no output pin).
- Interrupt Wake-up function
- Maskable Options for:
  - Low Voltage Detector (LVD)
  - Low Voltage Power Supply Supervisor (including Active Reset and LVD)
- IR Carrier Frequency Generator
- Master Reset and Power-On Reset
- 8-bit Data Manipulation
- 63 Basic Instructions
- 17 main Addressing Modes
- 8x8 Unsigned Multiply instruction
- True Bit Manipulation
- Complete Development Support on PC/DOS Real-Time Emulator
- Full Software Package (Cross-Assembler, Debugger)
- Full Hardware Emulator
- 16 and 32K EPROM and OTP support



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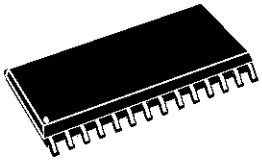

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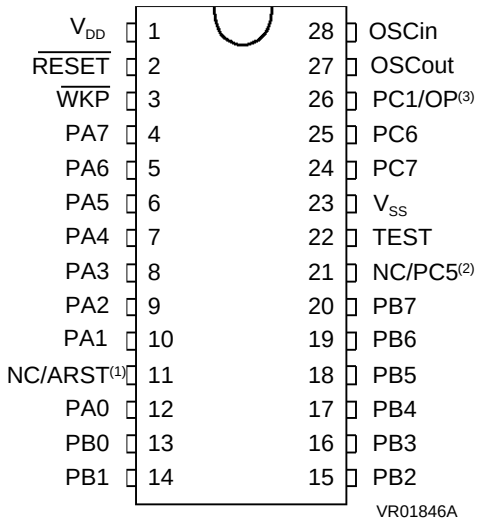
(See end of Datasheet for Ordering Information)

DEVICE SUMMARY

DEVICE	ROM (Bytes)	RAM (Bytes)	LVPSS (option)	CARRIER GENERATOR
ST7291C6(1)	32K	384	Yes	Yes
ST7291C5	24K	384	Yes	No
ST7291C4	16K	256	No	No

Note (1): This device is in development, consult your SGS-THOMSON representative for the current status.

Figure 1. Pin Description



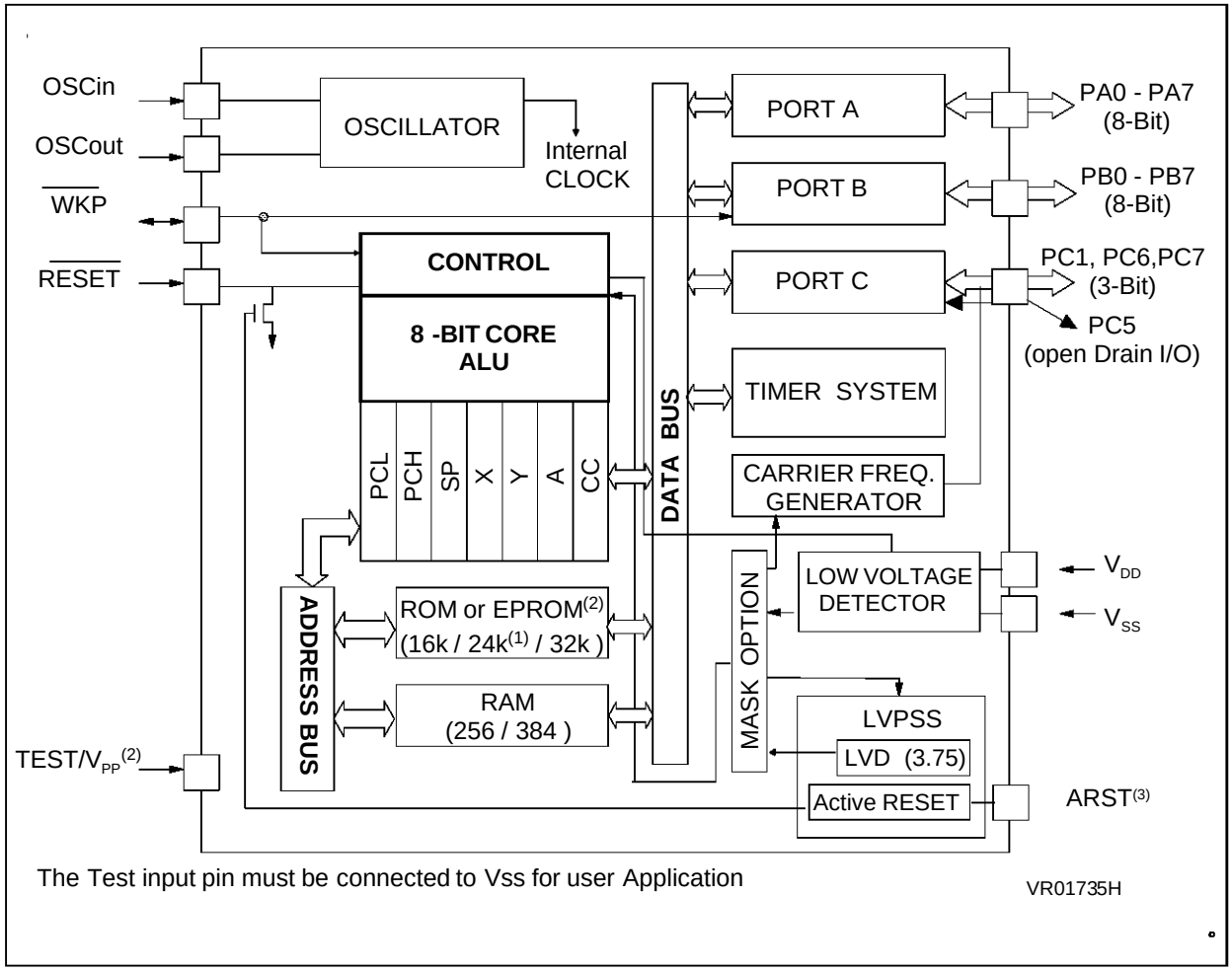
Notes:
1. Not connected (NC) on ST7291C4; ARST on ST7291C5/C6
2. Not connected (NC) on ST7291C4; PC5 on ST7291C5/C6
3. PC1 on ST7291C4/C5; software selectable as OP on ST7291C6

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST7291 HCMOS Microcontroller Unit is a member of the ST7 family of Microcontrollers. The device is based on an industry-standard 8-bit core and features an enhanced instruction set. The CPU may be driven by an external 8MHz clock when the device is operated with a 5V supply. Thanks to the fully static design, operation is possible down to DC. Under software control, the ST7291 may be placed in either WAIT or HALT modes, thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST7291 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes a CPU, ROM, RAM, I/O, an on-chip oscillator, a timer with output compare system and, depending on the version, options for Low Voltage Detection (LVD), Low Voltage Power Supply Supervision (LVPSS) and Carrier Frequency generation for remote control applications.

Figure 2. ST7291 Block Diagram



Notes:

1. ROM version only
2. EPROM version only
3. Present only in C5/C6 versions

1.2 PIN DESCRIPTION

V_{DD} Power supply.

V_{SS} Ground.

OSCin, OSCout Oscillator input and output pins. These pins are usually connected to a parallel resonant crystal or ceramic resonator. An external clock source may also be input via OSCin.

$\overline{\text{RESET}}$ An active-low input signal on this pin forces initialisation of the MCU. This is the highest priority interrupt and it is not maskable.

$\overline{\text{WKP}}$ This external software-maskable interrupt may be connected internally to PORTB via 30KΩ resistors by setting the WFD bit, in order to enable the PORTB wake-up function.

ARST Floating input pin to the LVPSS circuitry.

PA0-PA7, PB0-PB7, PC1, PC5, PC6, PC7 These 20 lines are standard I/O lines, programmable as either inputs or outputs.

– PORT A 8 standard I/O lines accessible via the DDRA and DRA registers;

– PORT B 8 standard I/O lines accessible via the DDRB and DRB Registers. The state of the WFD control bit determines whether PORT B will be a standard 8-bit I/O port or if it will be internally connected to the wake-up interrupt function;

– PORT C 3 standard I/O lines (PC7, PC6 and PC1) and one Open Drain I/O line (PC5), accessible via the DDRC and DRC Registers.

TEST This pin MUST be connected to the V_{SS} pin.

Table 1. ST7291 Pin Configuration

Name		Function	Description	Pin
7291C4	7291C5/C6			
V_{DD}	V_{DD}	I	Power Supply	1
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	I/O	Reset (Open-Drain I/O on C5/C6)	2
$\overline{\text{WKP}}$	$\overline{\text{WKP}}$	I/O	Wake-up Interrupt Signal	3
PA7	PA7	I/O	Standard Port	4
PA6	PA6	I/O	Standard Port	5
PA5	PA5	I/O	Standard Port	6
PA4	PA4	I/O	Standard Port	7
PA3	PA3	I/O	Standard Port	8
PA2	PA2	I/O	Standard Port	9
PA1	PA1	I/O	Standard Port	10
NC	ARST	I (analog)	LVPSS (Floating input to the Active Reset circuitry)	11
PA0	PA0	I/O	Standard Port	12
PB0	PB0	I/O	Standard Port (with Wake-up Interrupt facility)	13
PB1	PB1	I/O	Standard Port (with Wake-up Interrupt facility)	14
PB2	PB2	I/O	Standard Port (with Wake-up Interrupt facility)	15
PB3	PB3	I/O	Standard Port (with Wake-up Interrupt facility)	16
PB4	PB4	I/O	Standard Port (with Wake-up Interrupt facility)	17
PB5	PB5	I/O	Standard Port (with Wake-up Interrupt facility)	18
PB6	PB6	I/O	Standard Port (with Wake-up Interrupt facility)	19
PB7	PB7	I/O	Standard Port (with Wake-up Interrupt facility)	20
NC	PC5	I/O	Standard Port (Open-Drain)	21
Test	Test	I	Test (MUST be connected directly to the Vss pin)	22
Vss	Vss	I	Ground	23
PC7	PC7	I/O	Standard Port	24
PC6	PC6	I/O	Standard Port	25
PC1	PC1	I/O	Standard Port/ Pulse generator output (1)	26
OSCout	OSCout	O	Oscillator Output	27
OSCin	OSCin	I	Oscillator Input	28

Note1. PC1 on ST7291C4/C5, software selectable as OP on ST7291C6

1.3 MEMORY MAP

The major difference between the various versions of the ST7291 MCU is the User ROM memory addressing capability:

– C4 version: 15,840 bytes of User ROM
– C5 version: 24,160 bytes of User ROM
– C6 version: 31,456 bytes of User ROM

The C5 and C6 versions use the same User ROM addressing map beginning at address 01A0h and ending at 5FFFh for the C5 version, and ending at 7C7Fh for the C6 version. The C4 version uses a different addressing map, beginning at 0120h and ending at 3EFFh.

The first 32 bytes of RAM are reserved for the peripheral I/O registers. The User RAM space starts at the same address for all ST7291Cx versions. The ST7291C4 version can address up to 256 bytes of RAM, while the ST7291C5/C6 versions can address up to 384 bytes of RAM.

Figure 3. ST7291C5/C6 Memory Map

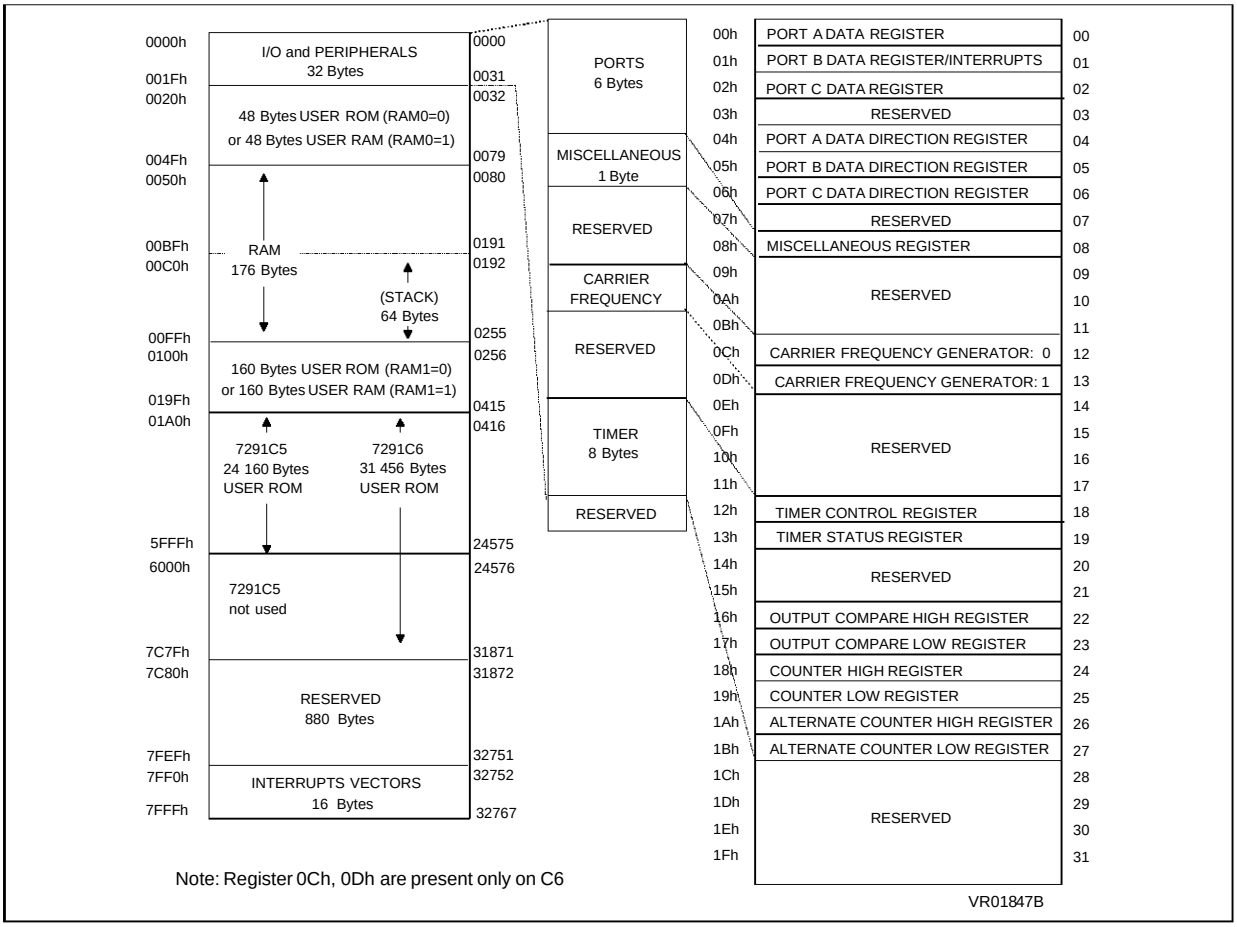


Table 2. ST7291C5/C6 Interrupt Architecture

Interrupt Class	Interrupt Generator(s)	Interrupt Source(s)	Interrupt Register	Vector Address
RESET	RESET / LVPSS	RESET / ARST Pins	none	7FFEh, 7FFFh
TRAP	USER PROGRAM	TRAP Instruction	none	7FFCh, 7FFDh
EXTERNAL	PORT B	WKP (Pin 3)	none	7FFAh, 7FFBh
TIMER	TIMER Value	OCF / TOF Flags	TIMER STATUS	7FF8h, 7FF9h
LVD	LVD Circuitry	LVDF Flag	MISCELLANEOUS	7FF6h, 7FF7h
RESERVED				7FF4h, 7FF5h
				7FF2h, 7FF3h
				7FF0h, 7FF1h

MEMORY MAP (Continued)

The interrupt vector matrix is similar for all ST7291Cx versions. It is located between addresses 7FF0h and 7FFFh on the C5/C6 versions, and between addresses 3FF0h and 3FFFh on the C4 version.

The RAM space includes 64 bytes for the stack, from address 00C0h to 00FFh. Programs that only use part of the allocated stack locations for interrupts and/or subroutine stacking, may address the remaining bytes as standard RAM locations.

Two areas of the memory map may be mapped either as RAM or as ROM depending on the state of the RAM0 and RAM1 flags of the Miscellaneous Register. The first of these two areas consists of 48 bytes for all Cx versions, the second area consists of 160 bytes on the C5/C6 versions and of 32 bytes on the C4 version.

Figure 4. ST7291C4 Memory Map

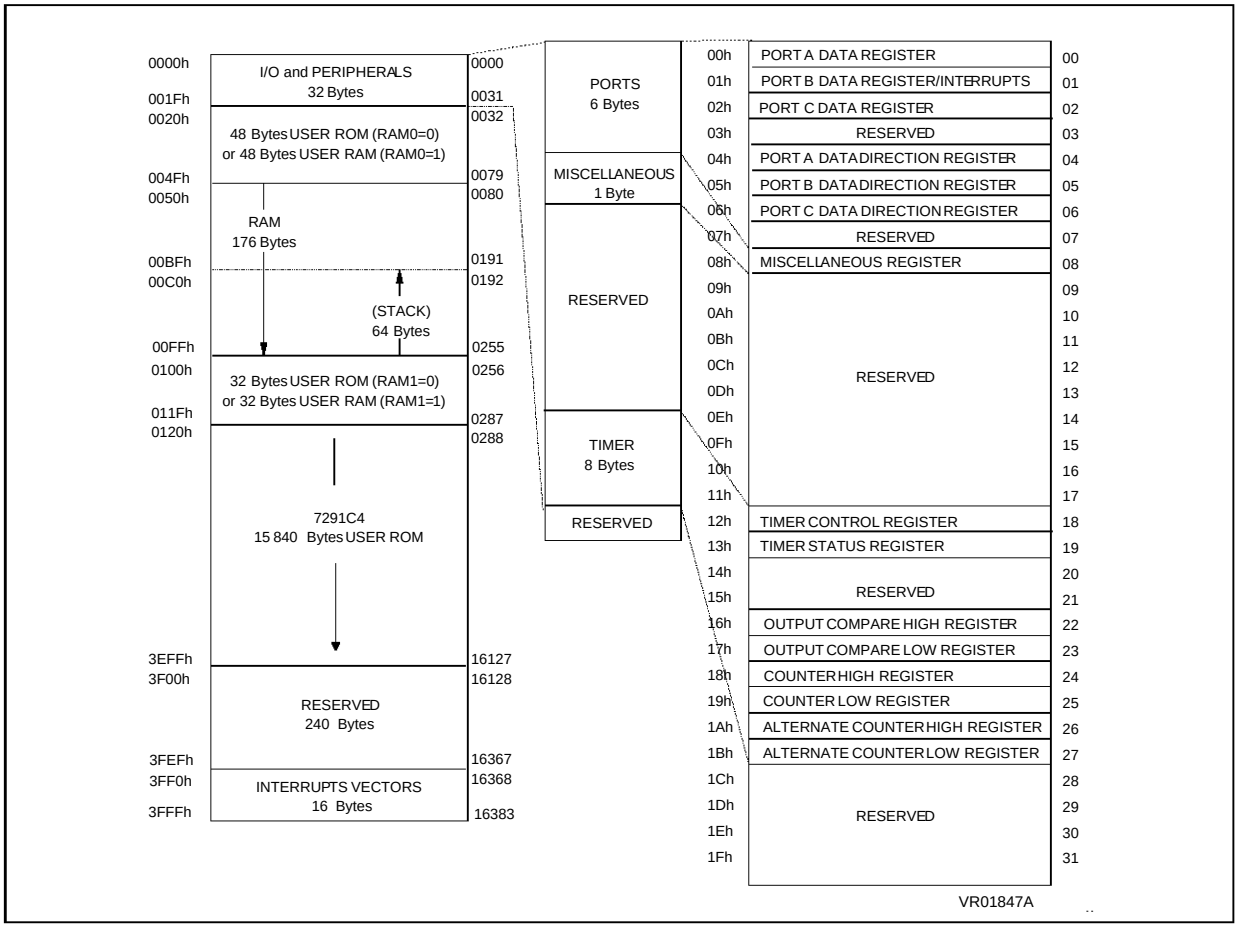


Table 3. ST7291C4 Interrupt Architecture

Interrupt Class	Interrupt Generator(s)	Interrupt Source(s)	Interrupt Register	Vector Address
RESET	RESET	RESET	none	3FFEh, 3FFFh
TRAP	USER PROGRAM	TRAP Instruction	none	3FFCh, 3FFDh
EXTERNAL	PORT B	WKP (Pin 3)	none	3FFAh, 3FFBh
TIMER	TIMER Value	OCF / TOF Flags	TIMER STATUS	3FF8h, 3FF9h
LVD	LVD Circuitry	LVDF Flag	MISCELLANEOUS	3FF6h, 3FF7h
RESERVED				3FF4h, 3FF5h
				3FF2h, 3FF3h
				3FF0h, 3FF1h

Notes: